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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/577,398	04/27/2006	Koichi Takeda	016778-0507	1397

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EXAMINER	
MAI, SON LUU	

ART UNIT	PAPER NUMBER
2827	

MAIL DATE	DELIVERY MODE
07/01/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/577,398	TAKEDA, KOICHI	
	Examiner	Art Unit	
	Son L. Mai	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) *12,28-41 and 45-48* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☒ Claim(s) *13-27,42-44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/27/06, 05/23/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

2. The Information Disclosure Statement papers filed 04/27/06 and 05/23/06 have been considered on the merits.

Election/Restrictions

3. Claims 12, 28-41, 45-48 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected inventions, there are no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 03/19/08.

Drawings

4. Figures 1-6 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The disclosure is objected to because of the following informalities:

On page 1, line 6 from the bottom of the page, the word “cash” should read –cache--.

On page 34, line 4 from the bottom of the page, "ad" should read --and--.

On page 40, line 4 from the top of the page, the word “input” should read –output--.

6. Claims 3, 8, 9, 10 and 43 are objected to because of the following informalities:

In claim 3, line 3, “a read and write bit line” should read –read bit line--.

In claim 8, line 2, an article “a” should be added before “second access transistor”.

In claim 9, line 3, “a read and write bit line” should read –read bit line--.

In claim 10, line 2, an article “a” should be added before “second access transistor”.

In claim 43, what does "memory cells inverted in mirror in three directions" mean? Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,808,933 issued to Ross, Jr. et al. (hereinafter ‘Ross’).

Regarding claim 1, Ross teaches a semiconductor memory device (see figure 5a) comprising: a memory cell (50) comprising first and second data storage nodes (nodes B and A), wherein the memory cell comprises: a first inverter circuit (consisting of transistors 60 and 66) including an input allocated to the second data storage node (node A) and an output allocated to the first data storage node, and a second inverter circuit (consisting of transistors 58 and 64) including an input allocated to the first data storage node (node B) and an output allocated to the second data storage node; and first access means (transistor 68) connected to the first data storage node for reading out data, and storage control means (transistor 56) serially connected to a drive transistor (58) of the second inverter circuit.

Regarding claim 2, Ross teaches a semiconductor memory device according to claim 1, wherein the memory cell further comprises second access means (transistor 62 in figure 5a) for accessing the second data storage node (node A), the second access means being activated with a write signal (signal 70) thereby performing data transfer between a write bit line (52) and the second data storage node.

Regarding claim 3, Ross teaches a semiconductor memory device according to claim 2, wherein the first access means (transistor 68 in figure 5a) is activated with a memory access signal (signal 72) thereby performing data transfer between a read bit line (54) and the first data storage node.

Regarding claim 4, Ross teaches a semiconductor memory device according to claim 3, wherein the first and second inverter circuits forming the memory cell includes a CMOS inverter circuit (58, 64 and 60, 66) and the first and second access means

(transistors 68 and 62) and the storage control means (transistor 56) include NMOS transistors.

Regarding claim 5, Ross teaches a semiconductor memory device according to claim 1, wherein the memory cell further comprises second access means (transistor 62) for accessing the second data storage node (node A) and the second access means is activated by a write signal 70) to reset the second data storage node.

Regarding claim 6, Ross teaches a semiconductor memory device according to claim 5, wherein the first and second inverter circuits forming the memory cell includes a CMOS inverter circuit (58, 64 and 60, 66) and the first and second access means (transistors 68 and 62) and the storage control means (transistor 56) include NMOS transistors.

Regarding claims 7-11, Ross teaches a semiconductor memory device having all the claimed limitations as shown in the rejection of claims 1-6.

Allowable Subject Matter

9. Claims 13-27 and 42-44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach at least the further limitations of the semiconductor memory device further comprising a sense amplifier including a bit line for transferring data to and from the memory cell, a data line for transferring data to and

from an input and output circuit, an inverter circuit including an input allocated to the bit line, data read means for transferring an output of the inverter circuit to the data line, and data write means activated by a write signal for transferring data from the data line to the bit line. In addition the prior art of record fails to teach the further limitation of claim 2, wherein elements forming the memory cell are placed in layout in an L-shaped region.

Conclusion

The prior art made of record cited on form PTO-892 is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on M-F from 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

06/26/08

/Son L. Mai/
Primary Examiner, Art Unit 2827